REMARKS

Claim 1 has been amended to specify that the layer of thermally insulating material and the layer of thermally conducting material extend across the whole area of the layer of electro-optic material; this amendment in effect incorporates the subject matter of claim 4 into claim 1. Accordingly, claim 4 has been cancelled as redundant over claim 1 as now amended. Claims 2, 3 and 5-10 are unchanged. Claim 11 has been amended to specify that an air gap present between the electrode and the layer of thermally conducting material, thus in effect incorporating the subject matter of claim 21 into claim 11. Claim 11 has further been amended to specify that the layer of thermally conducting material and the air gap extend across the whole area of the layer of electro-optic material; this amendment is based upon, *inter alia*, Figure 1, which shows the thermally conducting layer 108 and the air gap 110 extending over the whole area of the electro-optic material 102. Claim 21 has been cancelled as redundant over claim 11 as now amended. Claims 22-26 are unchanged.

No new matter is introduced by any of the foregoing amendments.

Claims 1-4, 7-11 and 22-25 stand rejected under 35 USC 103(a) as unpatentable over Duthaler, U.S. Patent No. 6,312,304, in view of Peterson et al., U.S. Patent No. 4,882,454. This rejection is traversed. More specifically, this rejection is traversed on the grounds that neither Duthaler nor Peterson describes an electro-optic display in which (a) a layer of thermally insulating material and a layer of thermally conducting material extend across the whole area of the layer of electro-optic material, with the layer of thermally conducting material being disposed between the layer of thermally insulating material and the layer of electro-optic material, as required by present claims 1-3 and 5-10; or (b) a layer of thermally conducting material and an air gap extend across the whole area of the layer of electro-optic material, as required by present claims 11 and 22-26.

Applicants concede that the summary of Duthaler appearing in the last three lines of page 2 and the first eleven lines of page 3 of the Office Action is essentially

correct. It is not entirely clear to applicants how the Examiner proposes to replace the single-sided circuit board 72 of Duthaler's Figure 6B (which for obvious reasons has chips disposed only on its surface facing away from the electro-optic medium 14) with the Peterson circuit board, which is inherently double-sided, with a thermally conductive core. More importantly, however, a combination of Duthaler and Peterson will not produce a display in accordance with any of the present claims. More specifically, such a combination of Duthaler and Peterson will not produce a display comprising a layer of thermally insulating material (hereinafter for convenience "an insulating layer") and a layer of thermally conducting material (hereinafter for convenience "a conducting layer") with the conducting layer being disposed between the insulating layer and the electro-optic layer *over the whole area of the layer of electro-optic material*, as required by present claims 1-3, 5-10 and 26, nor will such a combination produce a display having the air gap required by present claims 11 and 22-25.

With regard to claims 1-3, 5-10 and 26, the Office Action notes that the Peterson circuit board comprises a plurality of insulating layers and conducting layers, and both types of layers extend over the whole area of the board, so that if the Peterson board were used to replace the circuit board in Duthaler, these two layers would extend over the entire electro-optic layer. With regard to the requirement of claim 1 that the conducting layer be disposed between the insulating layer and the electro-optic layer, the Office Action directs attention to Figure 5 of Peterson, arguing that this Figure 5 shows one conducting layer 403 on the outer surface of the Peterson board so that this conducting layer would be disposed between the insulating layers and the electro-optic layer when the Peterson and Duthaler inventions were combined.

Applicants accept that Figure 5 of Peterson does indeed show one conducting layer 403 on the outer surface of the board such that this conducting layer 403 would lie between the insulating layers 402 and the electro-optic layer if the Peterson board were used in the Duthaler display. However, such a combination would not produce a conducting layer lying between the insulating layer and the electro-optic layer

over the whole area of the electro-optic layer, as required by present claim 1. Figure 5 of Peterson shows only a small proportion of the Peterson circuit board, namely the so-called thermal transfer region thereof, this region being designed to optimize transfer of heat from the core 102 of the board to the outside thereof (see column 4, lines 19-24 of Peterson). In this thermal transfer region, the vias short all of the conducting layers together so that it is necessary to pattern (as shown at 404) the conductive layers outside of the thermal transfer region, to ensure circuit definition integrity (see column 4, lines 28-32). In other words, as indicated at the right hand edge of Figure 5, the major part of the Peterson board does not have the structure shown in Figure 5 but rather than shown in Figure 1, with the major proportion of the external surface of the board occupied by an insulating layer rather than by a conducting layer. Accordingly, the combination of Duthaler and Peterson does not provide a conducting layer disposed between the insulating layer and the electro-optic layer over the whole area of the layer of electro-optic material, as required by present claims 1-3, 5-10 and 26.

With regard to claims 11 and 22-25, it is respectfully noted that claim 11 now incorporates the subject matter of former claim 21, which was not rejected over the combination of Duthaler and Peterson. Accordingly, it is believed that the Examiner will now accept that claims 11 and 22-25 are patentable over Duthaler and Peterson.

The 35 USC 103(a) rejection of claims 5 and 6 as unpatentable over Duthaler in view of Peterson and further in view of Leibowitz, U.S. Patent No. 4,812,792 is traversed for the same reasons as the rejection of claim 1 over Duthaler and Peterson alone, as discussed above.

The 35 USC 103(a) rejection of claims 21 and 26 as unpatentable over Duthaler in view of Peterson and further in view of Kawada et al., U.S. Patent No. 6,774,872, is traversed; this rejection is now presumably applicable to claim 11. More specifically this rejection is traversed on the grounds that Kawada is not properly combinable with the other two references.

The present claims are directed to displays using a layer of *reflective* electro-optic material. Kawada describes a plasma display panel (i.e., an emissive rather than reflective electro-optic display) the power drive circuitry of which consumes an electric power far greater than the electric power that is consumed by the drive circuit of a liquid crystal display (see column 1, lines 58-64 of Kawada). Kawada teaches that in view of the high power consumption of the power drive circuitry, the prior art arrangements shown in his Figures 2 and 3 result in excessive heating of the circuit board or glass substrate on which this circuitry is mounted, resulting in damage to the circuitry or possibly the plasma display panel itself (see column 3, lines 16-22). Kawada proposes as a solution to this problem mounting the power drive chip (42 in Kawada's Figure 10A) on a heat sink block (41) having an inner peripheral edge adjacent the peripheral edge of the substrate of the display and extending outwardly therefrom (see, for example, the last paragraph of Kawada's claim 1). Although Figure 10A does show other chips 45, 46 mounted on a printed circuit board 43 spaced from the display substrate 11 so that an air gap exists between the circuit board 43 and the substrate 11, there is nothing in Kawada to suggest that the chips on the circuit board are a significant source of heat likely to affect the display; the whole emphasis in Kawada is on dealing with the problems caused by the large heat generation in the chip 42. Furthermore, there is nothing in Kawada to suggest that the spacing between the circuit board 43 and the substrate 11 is intended to insulate the latter from the former; the presence of this "air gap" is apparently necessitated by the presence of the guide part 41A of the heat sink block 41 behind the substrate 11, the guide part 41A serving as a heat radiator (see column 6, lines 52-57 of Kawada discussing the very similar heat sink in Figure 5A).

Given the difference in power consumption between the electrophoretic display of Duthaler and the plasma display of Kawada, a person skilled in electro-optic displays would not consider Kawada relevant to the problem of heat dissipation in the Duthaler display. Furthermore, if the skilled person did wish to combine Duthaler and Kawada, the logical way to do so would be to move the drive circuitry of Duthaler from

its location behind the electro-optic medium to the edge of the display and heat sink the circuitry in the manner taught by Kawada. Finally, for the reasons noted above, Kawada does not teach any function for the air gap between the circuit board 43 and the substrate 11, this air gap apparently being an artifact of the type of heat sink used. Accordingly, Kawada would not teach the skilled person to incorporate such an air gap when incorporating the Peterson circuit board (which has nothing comparable to the Kawada heat sink) into the Duthaler display.

For all the foregoing reasons, the 35 USC 103 rejections in the Office Action are unjustified and should be withdrawn.

Since the prescribed period for responding to the Office Action expired November 29, 2006, a Petition for a two month extension of this period is filed herewith. The fees for this Petition, and for the Request for Continued Examination, are being paid concurrently with the filing of this Amendment.

Respectfully submitted
/David J. Cole/
David J. Cole
Registration No. 29629

E INK Corporation
733 Concord Avenue
Cambridge MA 02138

Telephone (617) 499-6069
Fax (617) 499-6200
E-mail dcole@eink.com